DELAYED LOCKED LOOP IMPLEMENTATION IN A SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY

ABSTRACT

A clock applying circuit for a synchronous memory is comprised of a clock input for receiving a clock input signal, apparatus connected to the synchronous memory for receiving a driving clock signal, and a tapped delay line for receiving the clock input signal and for delivering the clock driving signal to the synchronous memory in synchronism with but delayed from the clock input signal, the delay being a small fraction of the clock period of the clock input signal.